Remarks

Reconsideration of this Application is respectfully requested.

Claims 8-28 are pending in the application, with claims 8, 13, and 18 being the independent claims. Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Information Disclosure Statements

The Examiner has requested that Applicants supply "backup" copies of the references provided with the Fifth Supplemental Information Disclosure Statement filed on August 30, 2004. In accordance with the Examiner's request, copies of the references are submitted herewith.

Applicants also note that a Sixth Supplemental Information Disclosure Statement was filed in the present application on October 20, 2004 pursuant to 37 C.F.R. § 1.97(c). Applicants respectfully request that the Examiner initial and return a copy of the Form PTO-1449 enclosed with the Sixth Supplemental Information Disclosure Statement, and indicate in the official file wrapper of this patent application that the documents have been considered.

Obviousness-Type Double Patenting Rejections

The Examiner has rejected claims 8 and 9 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 29 of U.S. Patent No. 6,647,485, and claims 13 and 14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 35 of U.S. Patent No. 6,647,485. On December 15, 2004, in response to a telephonic request from the Examiner, Applicants filed in the present application a Terminal Disclaimer to Obviate a Double Patenting Rejection over U.S. Patent No. 6,647,485 and five other issued U.S. Patents[1], thereby rendering this rejection moot. Accordingly, Applicants respectfully request that the obviousness-type double patenting rejections of claims 8, 9, 13 and 14 be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 8-22 and 26-28 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,488,729 to Vegesna *et al.* ("Vegesna") in view of U.S. Patent No. 5,287,467 to Blaner *et al.* ("Blaner"). For the reasons set forth below, Applicants respectfully traverse.

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[1] The five other issued U.S. Patents are U.S. Patent Nos. 5,539,911; 5,689,720; 6,092,181; 6,038,654; and 6,256,720. In response to the Examiner's telephonic request, Applicants also filed a Terminal Disclaimer to Obviate a Provisional Double Patenting Rejection over co-pending U.S. Patent Application Nos. 10/282,045; 10/282,207; 10/283,177; 10/283,106; 10/660,671; 10/700,485; and 10/700,520.

Independent claim 8 is directed to a superscalar microprocessor for processing instructions having a sequential program order. Among other features, the claimed microprocessor includes:

> a resource identifying circuit configured to concurrently identify execution resources for a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including . . . a register file entry corresponding to a source of an operand for the instruction, [and]
>
> an issue control circuit coupled to the resource identifying circuit and configured to concurrently issue more than one of the available instructions to the functional units for execution, based on availability of the identified execution resources for each instruction and without regard to the sequential program order.

Vegesna does not teach or suggest at least the foregoing features of claim 8. In particular, Vegesna does not teach or suggest a resource identifying circuit that identifies a "register file entry corresponding to a source of an operand" for each instruction in an instruction buffer, and an issue control circuit that then issues an instruction "based on the availability" of the register file entry.

In Vegesna, during instruction scheduling, the two instructions stored in the DBUF (identified as the instruction buffer by the Examiner) are tested for two types of dependencies: "intrapacket dependencies", which are defined as data dependencies that exist between the two instructions stored in the DBUF (Vegesna, col. 26, ll. 32-35), and "interpacket dependencies", which are defined as data dependencies that exist between either one (or both) of the instructions currently in DBUF and those currently in certain processor pipeline stages (Vegesna, col. 26, ll. 35-41).

If an intrapacket dependency is detected, Vegesna's instruction scheduling logic delays the issuance of the second, dependent, instruction in the DBUF for a full processor cycle to allow the first instruction from which it depends to execute. *See,*

e.g., Vegesna, col. 35, ll. 43-46, col. 37, ll. 47-56, col. 38, ll. 35-40, col. 39, ll. 12-20. The dependency is then treated as an interpacket dependency (*see, e.g.,* Vegesna, col. 35, ll. 46-52) or some other specialized processing is performed. If an interpacket dependency is detected, Vegesna's instruction scheduling logic prevents the dependent instruction from issuing until it can obtain the result of the instruction from which it depends directly from a pipeline stage for use as an input (called "operand dependency bypass or forwarding circuitry"). Vegesna, col. 26, ll. 50-65. If neither dependency type is detected, the operands are accessed directly from the register file:

> If there are no interpacket dependencies, the appropriate functional unit input multiplexers (i.e. MuxC 18(c), MuxD 18(D), MuxA 20(A), MuxB 20(B), MuxStA 21 or MxStB 23) are directed by CSCHED 2 to select their inputs which emanate from IREGS 16; operands are accessed from the register file.

Vegesna, col. 26, ll. 50-55.

As demonstrated by the foregoing, Vegesna does not teach or suggest identifying a "register file entry corresponding to a source of an operand" for each instruction in the DBUF, and then issuing an instruction "based on the availability" of the register file entry. Rather, in Vegesna, if no data dependencies are detected, the scheduler simply assumes that the necessary operand data is available in the register file and issues the instructions; if there is an intrapacket dependency, the issuance of the dependent instruction is delayed for a cycle; and if there is an interpacket dependency, the result upon which the dependent instruction depends is provided directly from the pipeline stage in which the result is generated instead of from a register file. In each case, the timing of issuance is not "based on the availability" of a "register file entry corresponding to a source of an operand" identified for each instruction in the DBUF.

Blaner also does not teach or suggest this feature of claim 8. Blaner is directed to an architecture for a digital computer. The architecture includes a compounding preprocessor that determines if adjacent instruction in a stream of instructions can be executed in parallel. Based on compounding information provided from the compounding preprocessor, an instruction fetch and issue unit issues instructions either singly or in parallel. Blaner nowhere teaches or suggests that the instruction fetch and issue unit issues instructions "based on the availability" of a "register file entry corresponding to a source of an operand" identified for each instruction in an instruction buffer.

Since Vegesna and Blaner, alone or in combination, do not teach or suggest each and every feature of independent claim 8, they cannot render that claim obvious. Accordingly, the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that this rejection be withdrawn. Additionally, dependent claims 9-12 and 26 are also not rendered obvious by this combination for at least the same reasons as independent claim 8 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 9-12 and 26 under 35 U.S.C. § 103(a) is likewise traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Independent claim 13 is directed to a method for processing instructions having a sequential program order. Among other features, the method includes:

> concurrently identifying execution resources for more than one of a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including . . . a register file entry corresponding to a source of an operand for the instruction; [and]
>
> concurrently issuing more than one of the group of available instructions for execution by a plurality of functional units, based on

> availability of the identified execution resources for each instruction and without regard to the sequential program order.

The above-identified features of claim 13 are not taught or suggested by Vegesna or Blaner, alone or in combination, for the same reasons set forth above in regard to claim 1. Consequently, these references cannot render claim 13 obvious. Accordingly, the Examiner's rejection of claim 13 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that this rejection be withdrawn. Additionally, dependent claims 14-17 and 27 are also not rendered obvious by this combination for at least the same reasons as independent claim 13 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 14-17 and 27 under 35 U.S.C. § 103(a) is likewise traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Independent claim 18 is directed to a computer system. Among other features, the computer system includes:

> a resource identifying circuit configured to concurrently identify execution resources for a plurality of buffered instructions, the identified execution resources for each of the plurality of buffered instructions including . . . a register file entry corresponding to a source of an operand for the instruction, [and]
>
> an issue control circuit coupled to the resource identifying circuit and configured to concurrently issue more than one of the available instructions to the functional units for execution, based on availability of the identified execution resources for each instruction and without regard to the sequential program order.

The above-identified features of claim 18 are not taught or suggested by Vegesna or Blaner, alone or in combination, for the same reasons set forth above in regard to claim 1. Consequently, these references cannot render claim 18 obvious. Accordingly, the Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) is traversed and Applicants

respectfully request that this rejection be withdrawn. Additionally, dependent claims 19-22 and 28 are also not rendered obvious by this combination for at least the same reasons as independent claim 18 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 19-22 and 28 under 35 U.S.C. § 103(a) is likewise traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

The Examiner has rejected claims 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Blaner as applied to independent claims 8, 13, and 18 and further in view of U.S. Patent No. 5,317,720 to Stamm *et al.* ("Stamm"). As set forth above, the combination of Vegesna and Blaner does not render obvious claims 8, 13 or 18 because the combination fails to teach or suggest each and every feature of those claims. Stamm does not supply the missing teachings or suggestions. Therefore, the combination of Vegesna, Blaner and Stamm also cannot render independent claims 8, 13 or 18 obvious. Furthermore, dependent claims 23-25 are also not rendered obvious by this combination for at least the same reasons as the independent claims from which they respectively depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 23-25 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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